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ANALYSIS AND IMPLEMENTATION OF TRIVIAL DELAY BASED ADDERS

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ABSTRACT- In present-day, all digital devices are designed to be portable in which IC's are much compressed. When IC's turn into compacted ones, downsides in power and area get increased. Adders are requisite component for every contemporary Digital IC. A non-heuristic method for the analysis and optimization of adders with the intention of reducing delay is proposed here. Implementation with 20 different Boolean Expressions is done, which are constructed using CMOS logic and the performance is analyzed in terms of delay and area. This work is done with the Tanner EDA tool - 250nm technology. From this exploration the optimized equation is chosen to construct a full adder circuit in terms of multiplexer. These adders are incorporated in existing adder based circuits like BCD Adder, Array Multiplier, Booth multiplier, etc., and its performance is evaluated in terms of maximum combinational path delay and power.

INDEX TERMS- Boolean Expressions, BCD adder, Delay Calculation, Mux Based adders.

1 INTRODUCTION

An adder plays a vital role in many digital circuit designs including Digital Signal Processors (DSPs) and microprocessors. In electronics, an adder or summer is a digital circuit that performs addition of numbers. In modern computers adders reside in the arithmetic logic unit (ALU) where other operations are performed. Although adders can be constructed for many numerical representations, such as Binary-coded decimal or excess-3, the most common adders operate on binary numbers. Most of the VLSI applications like Digital Signal processing, video and image processing and microprocessors extensively use arithmetic operation. Thus adders form the basic part for most of the applications. In all kind of digital IC's the transistor sizes are reduced to make the device portable. Making these devices more and more compact lead to the increase in delay and power. Delay forms the most important part of the device operation. Increased delay affects the overall performance. Lesser the delay, higher is the performance.

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The simplest gate delay model sets a fixed propagation time, or gate delay Td, from a gate input to a gate output. Propagation delay is a technical term that can have a different meaning depending on the context. In electronics, the propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. Often this refers to the time required for the output to reach from 10% to 90% of its final output level when the input changes. Reducing gate delays in digital circuits allows them to process data at a faster rate and improve overall performance. Logic gates that compute other functions require more transistors, some of which are connected in series, making them poorer than inverters at driving current. Thus a NAND gate must have more delay than an inverter with similar transistor sizes that drives the same load. The method of logical effort quantifies these effects to simplify delay analysis for individual logic gates and multi-stage logic networks.

Various approaches have been made till date to reduce the delay in most of the circuits. Especially the adders with reduced delay will assist more in the performance escalation. Some of the different approaches made till date are discussed in the next section.

2 EXISTING TECHNIQUE

2.1 GDI TECHNIQUE

The circuit operation of GDI Based Full Adders is exactly the same as that of previous SERF module. Sum bit is obtained from the output of the second stage of XOR and XNOR circuit while Carry bit (Cout) is calculated by multiplexing B and Cin controlled by (A XNOR B). The main advantage of this technique is that which is having two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without huge amount of transistor count. The major problem of a GDI cell is that it requires twin-well CMOS or silicon on insulator (SOI) process to realize. Thus, it will be more expensive to realize a GDI chip. Moreover if only standard p-well CMOS process is used, the GDI scheme will face the problem of lacking driving capability which makes it more expensive and difficult to realize as a feasible chip.

2.2 STATIC ENERGY RECOVERY FULL ADDER

In this type of adder the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. The cout can be calculated by multiplexing a and cin controlled by (a $\otimes$ b). Let us consider that there is a capacitor at the output node of the first XNOR module. To illustrate static energy recovery let us consider an example where initially **a=b=0** and then a changes to 1. When a and b both equals to zero the capacitor is charged by VDD. In the next stage when **b** reaches a high voltage level keeping a fixed at a low voltage level, the capacitor discharges through a. Some charge is retained in a. Hence when a reaches a high voltage level we do not have to charge it fully. So the energy consumption is low here. The main drawback is that circuit produces full-swing at the output nodes. But it fails to provide so for the internal nodes. As the power consumption by the circuit reduces the circuit becomes slower. Also it cannot be cascaded at low power supply due to multiple threshold problems.

2.3 MINORITY FULL ADDER

MinFA is a Minority based Full Adder which has 34 Transistors. Although this low-power CMOS based design is modular, it has a long critical path and not a high driving capability at Sum output node, which leads to long propagation delay.

2.4 INVERTER BASED FULL ADDER

InvFA is an Inverter based Full Adder it has seven capacitors and four inverters. The main advantage of this design is its simplicity, modularity and low number of transistors. Although it has driving capability at the output nodes, its relatively long critical path results in long delay.

2.5 BRIDGE STYLE

BCFA which is designed based on the low-power CMOS Bridge style and Capacitors network includes four capacitors and 12 transistors. Besides its low power consumption, low driving power of the bridge circuit to the 2C capacitor and the inverter, which generate Cout, increase the delay of the circuit. Finally, this design produces complementary outputs and needs two additional inverters at the output nodes. In Proposal work,using different Boolean expression for a one-bit full adder gives effective result than these existing one. In Section III, gives the proposed method.Simulation and Results in Section IV,Future Work in Section V and Conclusion in Section VI.

3 PROPOSED FULL ADDER DESIGN

As very well known,adders form mandatory component of every current Integrated circuits for example consider Ripple carry adder,carry select adder,etc all has the use of full-adder,If any one of the full-adder gets a drawback it affects the whole circuit.So optimization of full-adder is carried out here.It is done by constructing 20 different Boolean expressions that are constructed in cmos logic and performance is analysed

Digital circuits use ON-OFF devices to implement operations of a system of logic called TWO-VALUED using BOOLEAN EXPRESSION. The statement may take the form of algebraic expressions, logic block diagrams, or truth tables, as well as circuits.Boolean expression is composed of variables and terms.The simplification of Boolean expression can lead to more effective computer programs, algorithms and circuits.

FORMS OF BOOLEAN EXPRESSIONS

1 SUM OF PRODUCT FORM (SOP) :

W=(X\` Y\` Z\`) + (X\` Y Z\`) + (X\` Y\` Z)

Each term in such an expression is called **minterm.**

Minterm : It is obtained from an AND term of n variables with each variable being primed, if corresponding bit of binary number is 0 and unprimed, if it is 1.

2 PRODUCT OF SUM (POS):

S=(P + Q + R) (P+ Q\` + R) (P\`+ Q + R)

Each term in such an expression is called **maxterm.**

Maxterm : It is obtained from an OR term of n variables with each variables being unprimed, if corresponding bit is a 0 and primed if it is 1.

MINIMIZATION OF BOOLEAN EXPRESSION

- Convert equation from POS form to SOP form.
- Remove parenthesis if any in the expression.
- If there are two or more identical terms,keep only one of them and drop the other.
- If a variable and its complements are present in a term,reduce it to 0. (A. A\`=0).
- Group two terms of which one contains a variable and other its complement, except for which both are identical. They can be reduced to a single term and in the reduced term, above variable will be absent (C + C\` =1).e.g. ; (A .B C\`) + (A. B. C)=A.B(C\` + C)=A.B
- If there are two terms which are identical except that one contains an extra variable, reduce them into a single term by dropping the larger one.e.g: B.C + A\`. B. C=B . C(1 + A\`)=B . C(1) = B . C

With this method, 20 different full adders are designed and their equations are as follows:

- $SUM = A \oplus B \oplus C$
- $SUM = \overline{A \oplus B \oplus C}$
- $SUM = \overline{(\overline{A}B + \overline{B}A)C} + (\overline{A}B + A\overline{B})\overline{C}$
- $SUM = \overline{(\overline{A}\,\overline{B} + AB)}\,\overline{C} + (\overline{A}\ \overline{B} + \text{AB})$
- $CARRY = (A \oplus B)C + AB$
- $CARRY = \overline{\overline{(A \oplus B)}}\,C + AB$
- $CARRY = (\overline{\overline{AB} + (\overline{A \oplus B})\overline{C}}$
- $CARRY = \overline{\overline{AB}\,.\overline{AC}\,.\overline{BC}}$
- $CARRY = \overline{A \oplus B} \cdot B + A \oplus B\,.C$
- $CARRY = \overline{\overline{(A \oplus B)\,.C} \oplus \overline{AB}}$
- $CARRY = C\,.(A\,.B) + C\,.(A + B)$
- $CARRY = AB + AC + BC$
- $CARRY = \overline{\overline{(A \oplus B)C}\,.\overline{AB}}$
- $CARRY = AB + \overline{\overline{A \oplus B}}\,.C$
- $CARRY = \overline{\overline{AB\,.\ AC\,.BC}}$
- $CARRY = \overline{\overline{\overline{A \oplus B}}\,.\overline{AC}\,.\overline{BC}}$
- $CARRY = \overline{\overline{AB}\,.\overline{\overline{\overline{A + B}}\,.C}}$
- $CARRY = \overline{\overline{\overline{A \oplus B}}\,.C \oplus \overline{\overline{AB}}}$
- $CARRY = \overline{\overline{A} + \overline{B}} + \overline{\overline{A \oplus B} + \overline{C}}$
- $CARRY = \overline{\overline{(\overline{A \oplus B})\,C \oplus \overline{AB}}}$

All these expressions are designed using CMOS in Tanner and delay is measured.Result showed that full adder with XOR-MUX had the lowest delay and power.The delay and power results are represented in Table 1.BCD adder is designed in Tanner by replacing the full adder in the original circuit with few of these different adders and delay was measured and compared.Results show that a BCD adder with XOR-MUX based full adder had lesser delay than the same circuit with other different full adder.An example circuit with XOR-AND-OR(1) based BCD adder and the XOR-MUX based BCD adder is represented in Fig 1& 2.Their delay measurement is also shown in the Table 2

4 SIMULATION AND RESULTS

The simulation results are shown in Table 1.The performance of all the full adders has been analyzed in terms of delay and transistor count.

TABLE 1
SIMULATION RESULTS OF DIFFERENT ADDERS

FULL ADDER USING	DELAY (ps)	AREA
XOR,AND,OR	36.1	38
XNOR,AND,OR	33.1	30
XNOR,AND,OR,NOT	34	32
XOR,AND	36.2	30
XOR,NAND,NEG OR	30.13	30
XNOR,NAND,NOT	29.5	34
XNOR,NAND	23.01	30
XOR,NAND	23.042	30
XOR,MUX	**18.02**	**18**
XNOR,MUX,NOT	19.01	20
XOR,XNOR,MUX	20.8	24
XOR,AND,OR,MUX	23.6	30
XNOR,AND,OR,MUX	26.12	30
NAND	20.2	36
NOR	40.1	51
XOR,NAND,NOR,NOT	32.2	38
XNOR,NAND,NOR,NOT	31.1	38
XNOR,NOR,NOT,OR	34.1	40
XOR,NOR,NOT,OR	35	42
XOR,AND,OR(2)	33.1	30

The least delay adder with XOR-MUX based is incorporated in BCD adder.Thus Fig.1 and Fig.2 Shows BCD adder with higher delay and BCD adder with lesser delay respectively.
The adder that has lesser delay shows,the use of XOR-MUX based adder and also the other few adders are also used and compared.

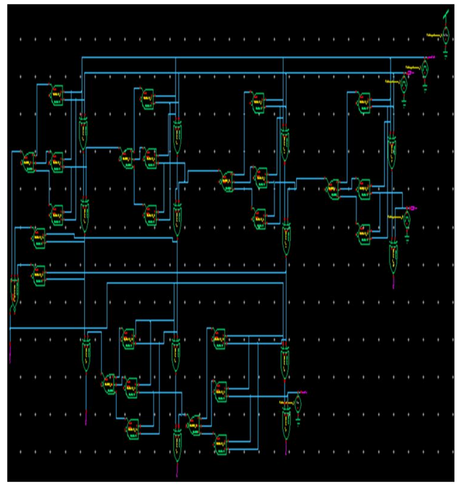

Fig.1 BCD ADDER USING XOR,AND,OR

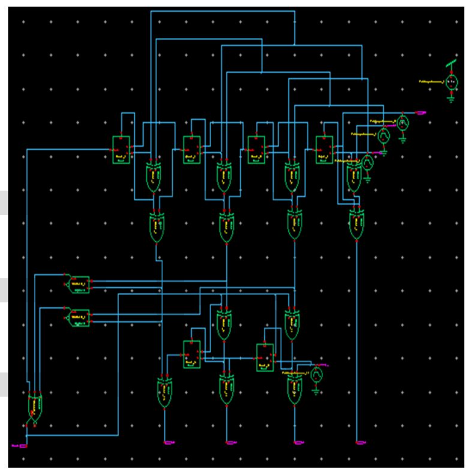

Fig.2 BCD ADDER USING XOR-MUX

COMPARISON AND RESULT

TABLE 2
COMPARISON RESULTS

BCD ADDER USING	DELAY (ns)
XOR,AND,OR(1)	300.1116n
XOR,MUX	**198.700n**
XOR,NOR,NOT,OR	200.111n
XOR,AND	299.133n
NOR	400.111n

5 FUTURE WORK

These different adders is implemented in higher applications like Booth multiplier,Array multiplier,etc.To show that adder using XOR-MUX gives the lesser delay,area and power when compared with the other adders.

6 CONCLUSION

Delay is the time required for the output to reach from 10% to 90% of its final output level when the input changes. Reducing gate delays in digital circuits allows them to process data at a faster rate and improve overall performance. The proposed 20 different Boolean expression are simulated using Xilinx ISE 9.1 Tool. Delay for all the adders are calculated and the final result shows that MUX based adders have lesser delay.When implementin those different adders in BCD adder shows the result that the adder using XOR-MUX shows the least delay and thus comparison and simulation is presented.

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